APA in view of Wu, Cho et al., and Kawachi et al. (U.S. Patent 6,104,040). The Office Action also rejected claims 18 and 19, as being unpatentable over APA in view of Wu, Cho et al., and Nakajima et al. (U. S. Patent 6,118,140). The Office Action rejected claim 20 under 35 U.S.C. 103, as being unpatentable over APA in view of Wu, Cho et al., and Gardner et al. (U.S. Patent 5,872,376). Applicant has amended independent claim 15 above, to improve clarity. After entry of the foregoing amendments, claims 15-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a thin film transistor has an ultra thin polysilicon layer over a substrate, a gate structure that includes a gate layer, a gate oxide layer between the gate layer and the ultra thin polysilicon layer and a spacer on each sidewall of the gate layer, and a conductive layer over the ultra thin polysilicon layer and the gate layer adjacent to the spacers. A selective deposition, such as an in-situ silicon-germanium deposition that utilizes the difference in properties between the spacer and silicon, is conducted to form the conductive layer serving as a S/D region without additional implantation process.

Discussion of Office Action Rejections

Applicant has amended claim 15 to recite the features as described in Page 6. No new matter adds by way of these amendments.

The Office Action rejected claims 15 and 16 under 35 U.S.C. 103, as being unpatentable over Applicant's Prior Art (APA) in view of Wu and Cho et al.. In addition, the Office Action

rejected claim 17 under 35 U.S.C. 103, as being unpatentable over APA in view of Wu, Cho et al., and Kawachi et al.. The Office Action also rejected claims 18 and 19, as being unpatentable over APA in view of Wu, Cho et al., and Nakajima et al.. The Office Action rejected claim 20 under 35 U.S.C. 103, as being unpatentable over APA in view of Wu, Cho et al., and Gardner et al.. Applicant respectively traverses the rejections for at least the reasons set forth below.

As had discussed in the previous response, in FIG. 2C of the present invention, the spacer 208 with respect to the gate electrode 206 and the polysilicon layer 202 forms a contrast surface, which allows the conductive layer 210 to be selectively formed on the polysilicon 202 and the gate electrode 206 but not on the spacer. Also and, the conductive layer 210 can serve as the source/drain region without additional implanting process of the dopants into the source/drain region. As a result, the fabrication process can be reduced.

Independent claim 15 recites the features as follows:

> 15. A thin film transistor structure, comprising:
> an insulating substrate;
> a polysilicon layer over the substrate;
> a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer, ***wherein the spacer with respect to a surface of the gate dielectric layer and a surface of the polysilicon layer forms a contrast surface;*** and
> ***a selective conductive layer over the gate layer and the polysilicon layer adjacent to the spacers based on the contrast surface, wherein the selective conductive layer adjacent to the spacers serves as a source/drain region without additionally implanting process on the source/drain region***. (*Emphasis added.*)

The features emphasized in amended claim 15 are at least not disclosed by the prior art references.

In re APA, APA failed to disclose the emphasized features in claim 15.

In re Wu, even though a spacer 24 is formed, however the doped spacer 24 together with the doped conductive layer 26 are used to form the source/drain region in the substrate (col. 4, lines 61-65) by thermal diffusion. The spacer of the 208 of the present invention has different function from the spacer 24 disclosed by Wu. The two spacers with respect to the present invention and Wu are not equivalent.

In re Cho et al. (col. 4, lines 53-55), the additional implanting process is used to inject impurity ions into the semiconductor layer 14 with an inclination angle, so as to form the source/drain regions. The semiconductor layer 14 is not selectively formed on a polysilicon layer but blankly on the gate insulation film 13. Therefore, the semiconductor layer 14 is also not equivalent to the conductive layer 210 of the present invention. ***It should be noted that the conductive layer 210 of the present invention is selectively form on the polysilicon layer 202 (but not the insulation layer 13 for Cho et al.)***. Also and, ***the present invention needs no the additional implanting process.***

When considering the present invention as a whole, the contrast surface between the spacer 208 and the polysilicon layer 202 is created and used to form the conductive layer 210, which serves as the source/drain region without additional implanting process. The present invention as recited in independent claim 15 has not disclosed by APA in view of Wu and Cho et al..

In re Kawachi et al., Nakajima et al., and Gardner et al., even though materials of the conductive layer is disclosed, however, these prior art references failed to supply the missing

feature about the conductive layer on the polysilicon layer (channel layer) serving as the source / drain region.

When considering the present invention as a whole, the prior art references either alone or in combination failed to disclose the features as recited in independent claim 15 and claims 16-20.

Further still, it seems that the hindsight has been used to pick the structure elements up piece by piece without base on their specifically original disclosure in the prior art. Applicant respectfully requests that the hindsight should be avoided.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 15 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 16-20 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 15-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW WHERE CHANGES MADE

In The Claims

Please amend claim 15 as follows:

15. (Twice Amended) A thin film transistor structure, comprising:

an insulating substrate;

a polysilicon layer over the substrate;

a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer, wherein the spacer with respect to a surface of the gate dielectric layer and a surface of the polysilicon layer forms a contrast surface; and

a selective conductive layer over the gate layer and the polysilicon layer adjacent to the spacers based on the contrast surface, wherein the selective conductive layer adjacent to the spacers serves as a source/drain region without additionally implanting process on the source/drain region.